

FIG. 1

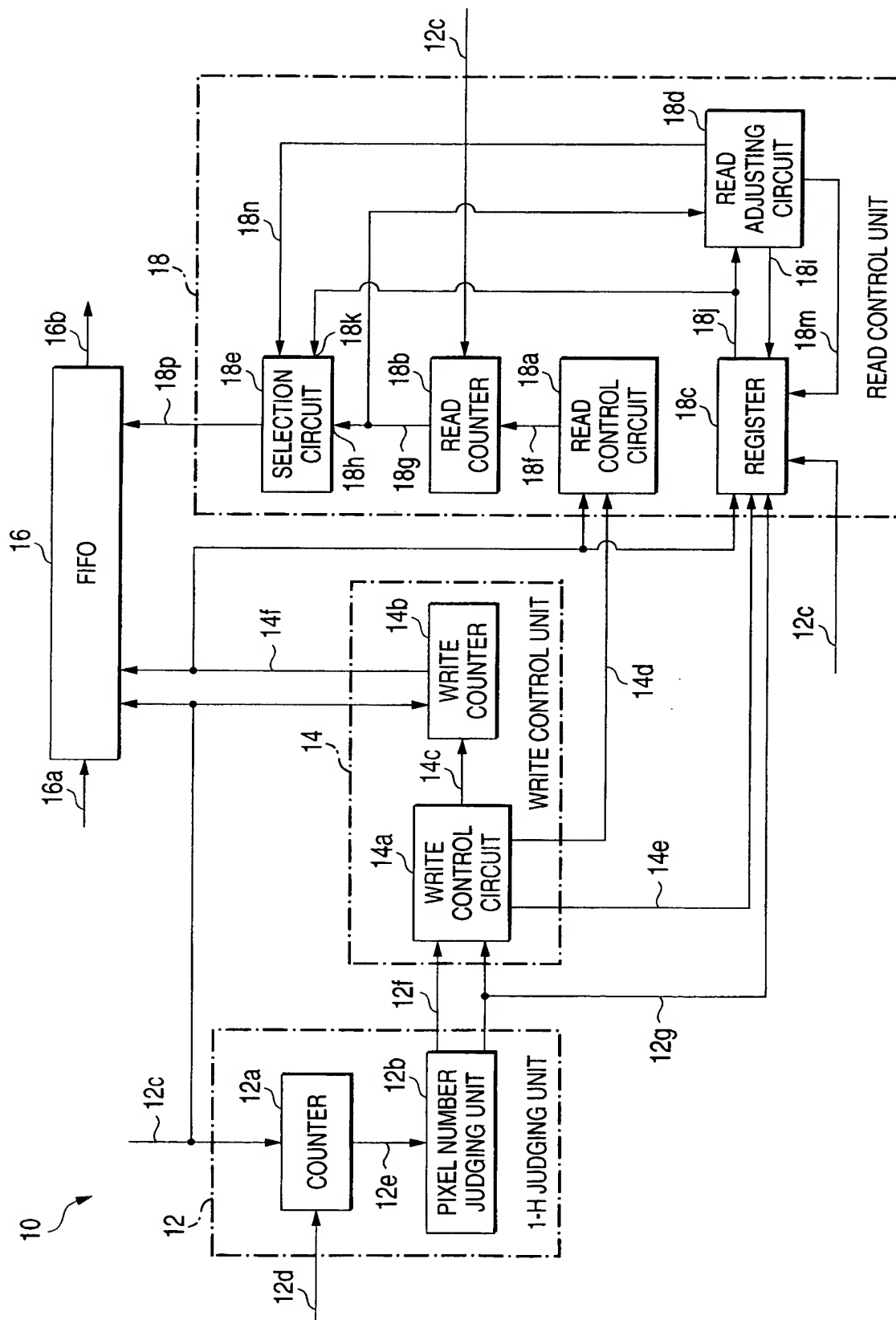
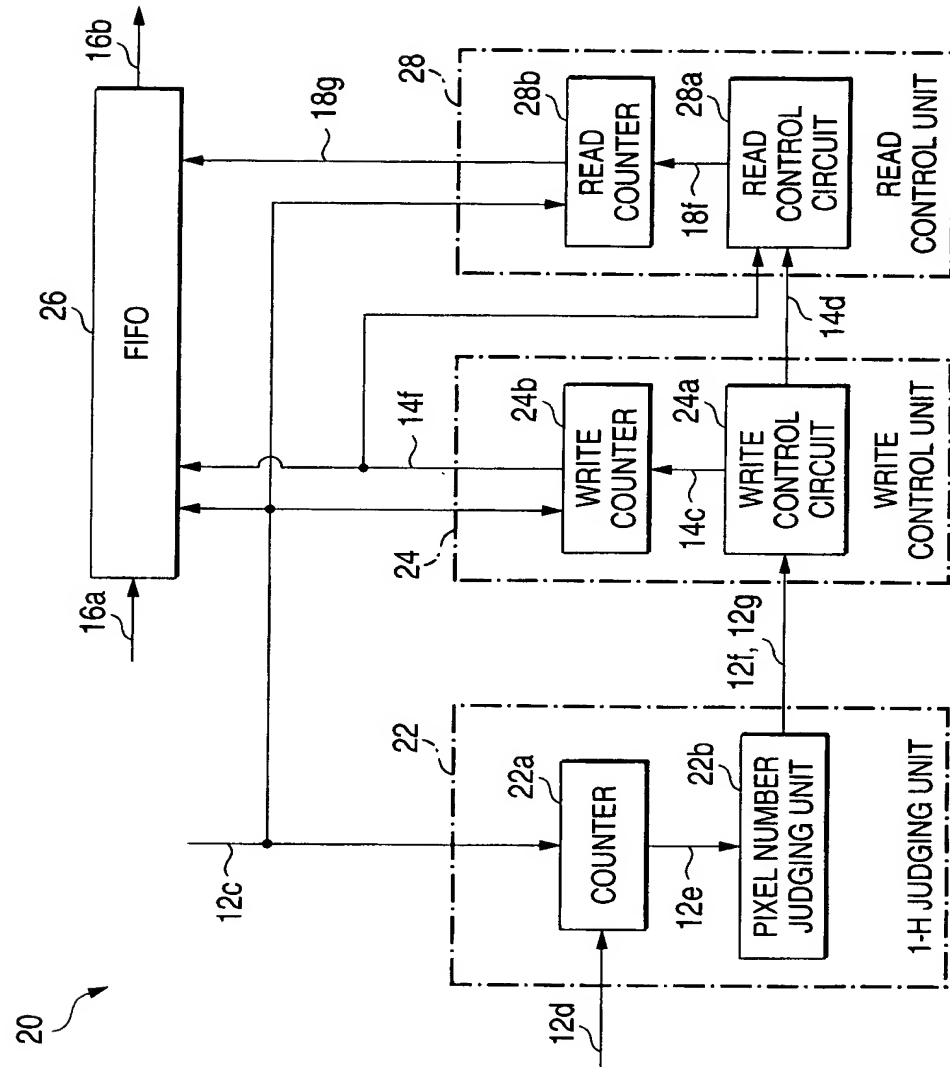
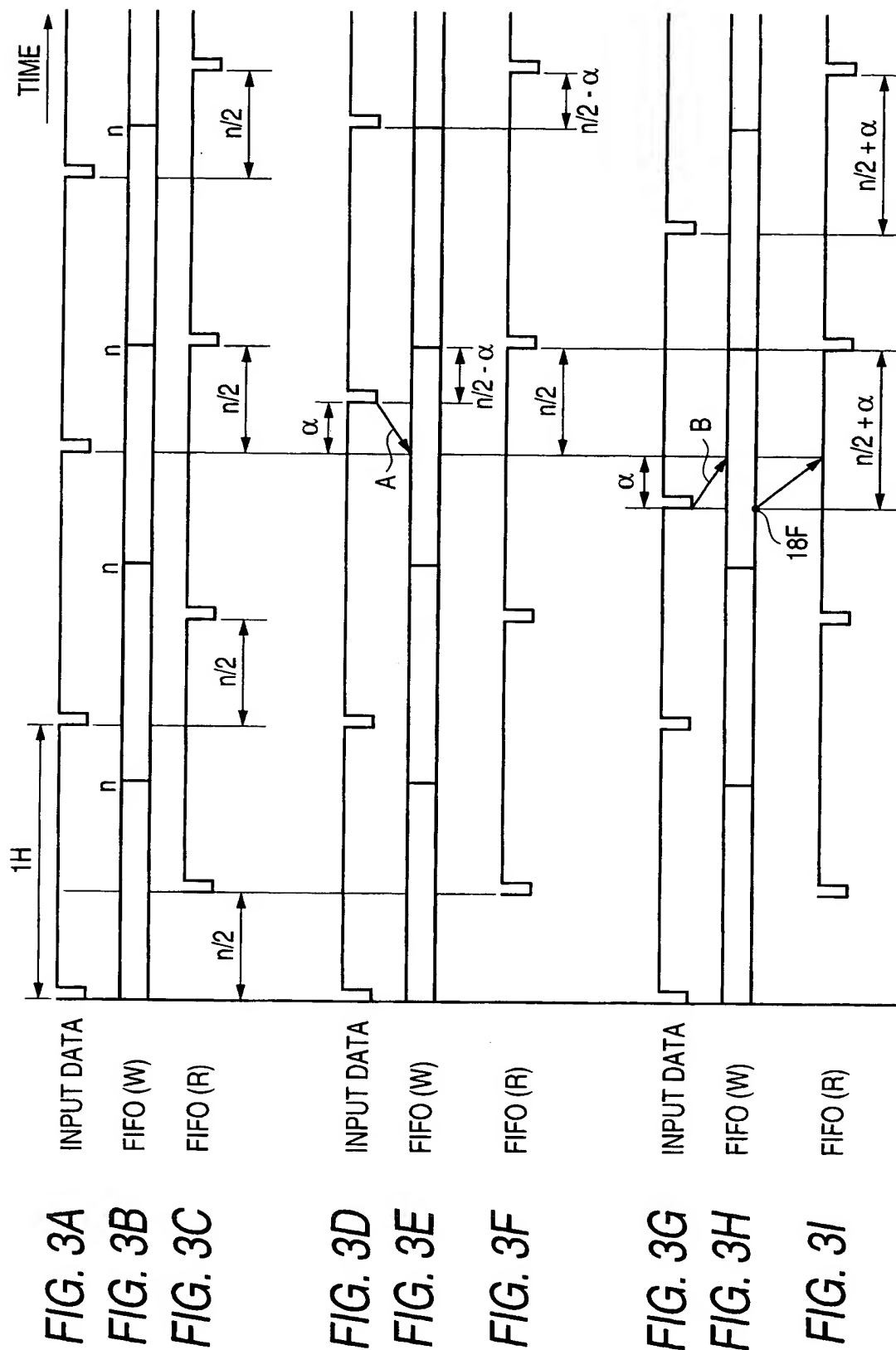


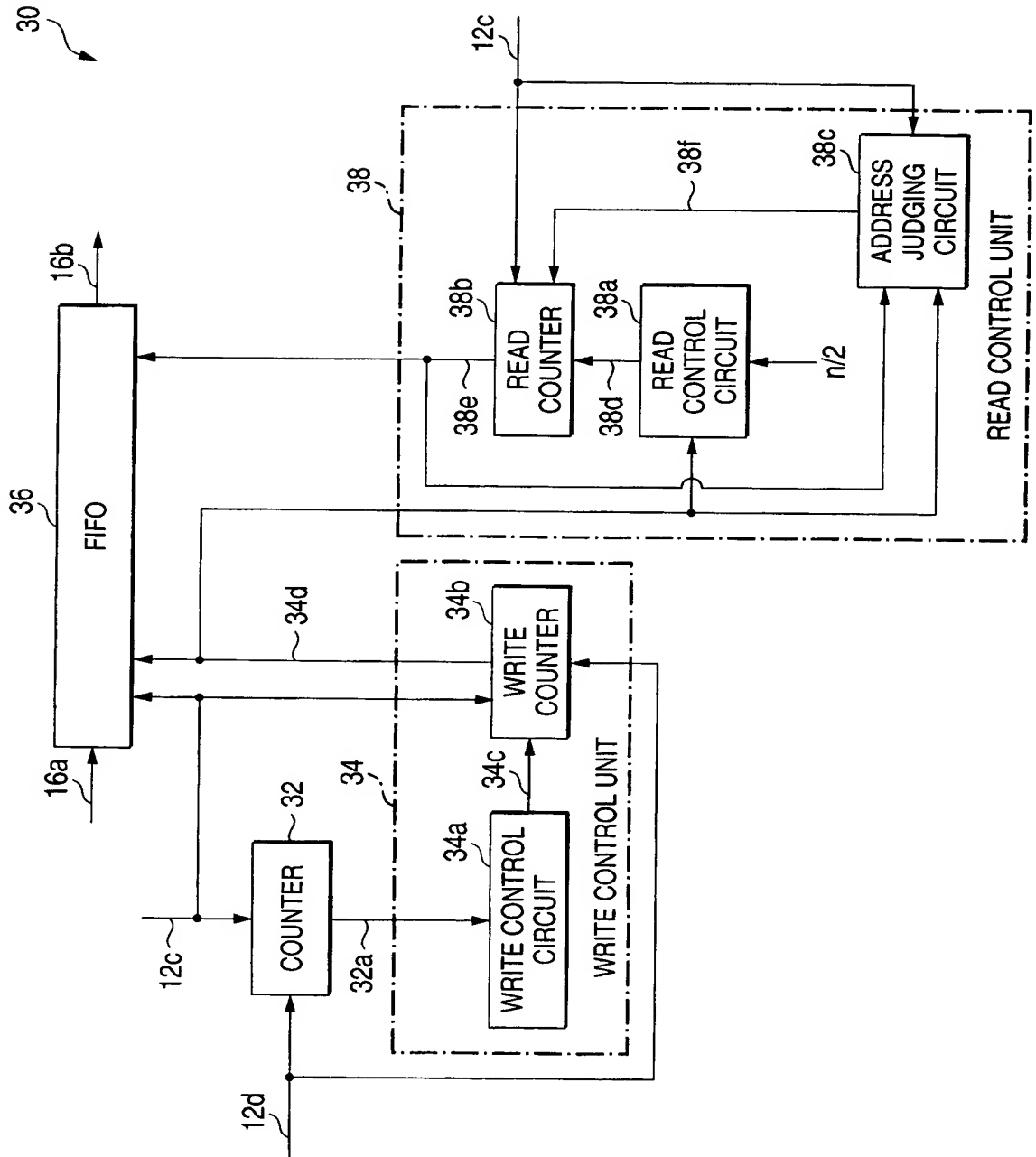
FIG. 2





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FIG. 4



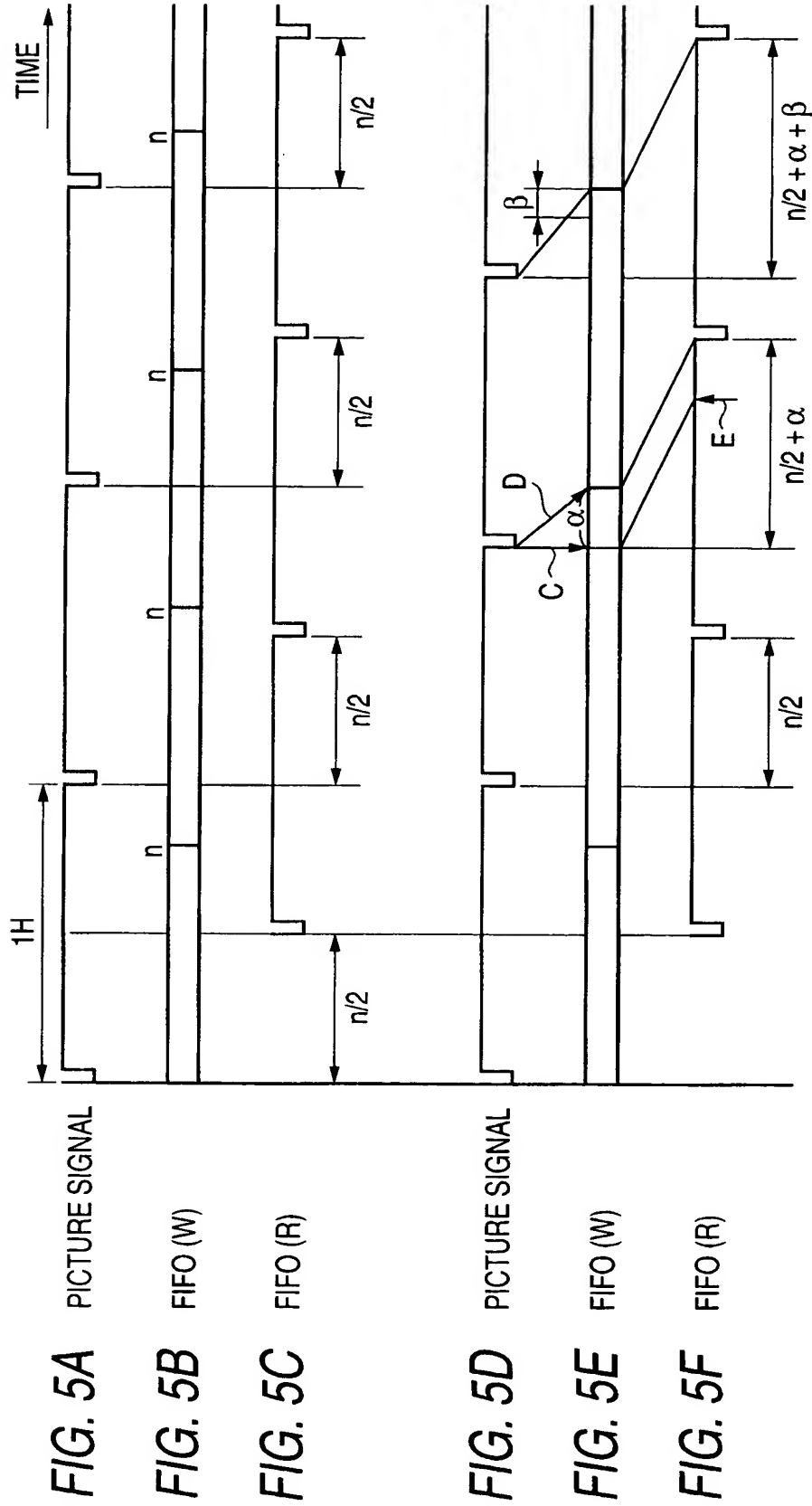
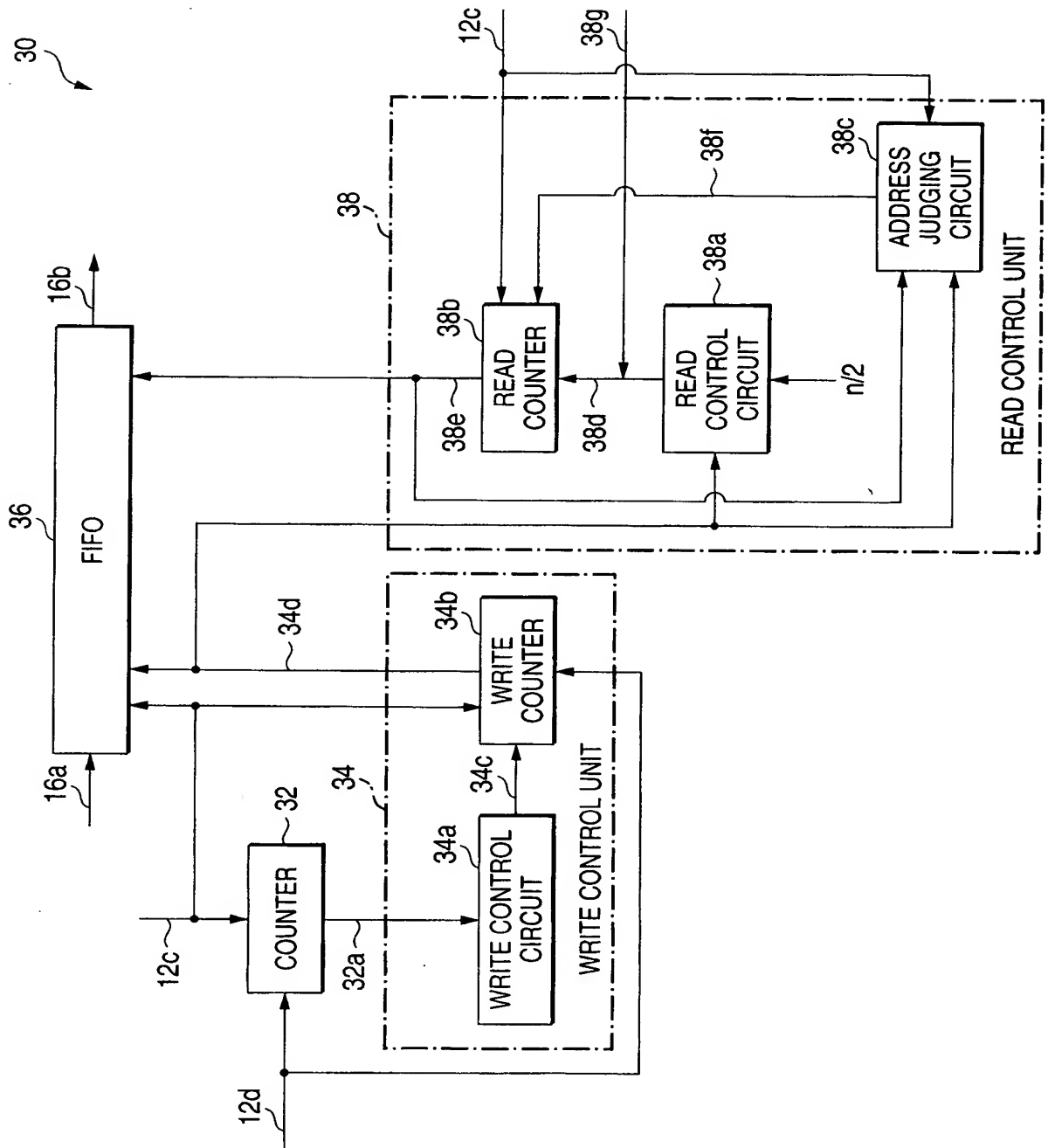


FIG. 6



The diagram illustrates a data transfer system 30. It features a FIFO (First In, First Out) buffer 36 with input 16a and output 16b. A counter 32 is connected to the input of the FIFO. The system is divided into two main control units: a WRITE CONTROL UNIT 34 and a READ CONTROL UNIT 38. The WRITE CONTROL UNIT 34 includes a WRITE CONTROL CIRCUIT 34a and a WRITE COUNTER 34b. The READ CONTROL UNIT 38 includes a READ CONTROL CIRCUIT 38a and a READ COUNTER 38b. An ADDRESS JUDGING CIRCUIT 38c is also part of the READ CONTROL UNIT 38. The system is controlled by signals 12c and 12d. Signal 12c is connected to the counter 32 and the read counter 38b. Signal 12d is connected to the write counter 34b and the read counter 38b. The FIFO 36 is connected to the read counter 38b and the write counter 34b. The read counter 38b is connected to the read control circuit 38a, which is connected to the address judging circuit 38c. The write counter 34b is connected to the write control circuit 34a, which is connected to the address judging circuit 38c. The address judging circuit 38c is connected to the read control circuit 38a and the write control circuit 34a.

FIG. 8

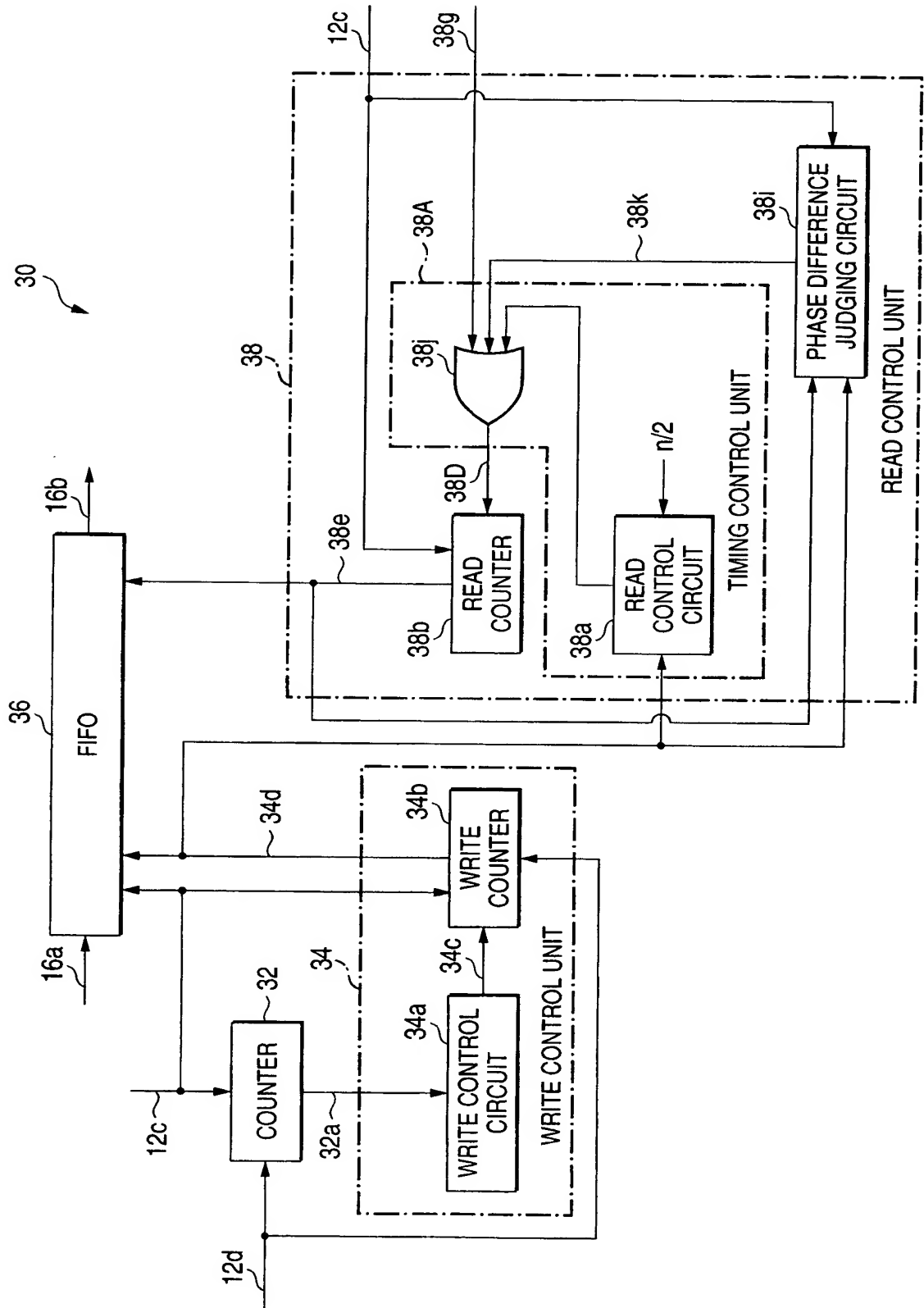




FIG. 9

